



74VHC16240

16-BIT BUS BUFFER WITH 3-STATE OUTPUTS (INVERTED)

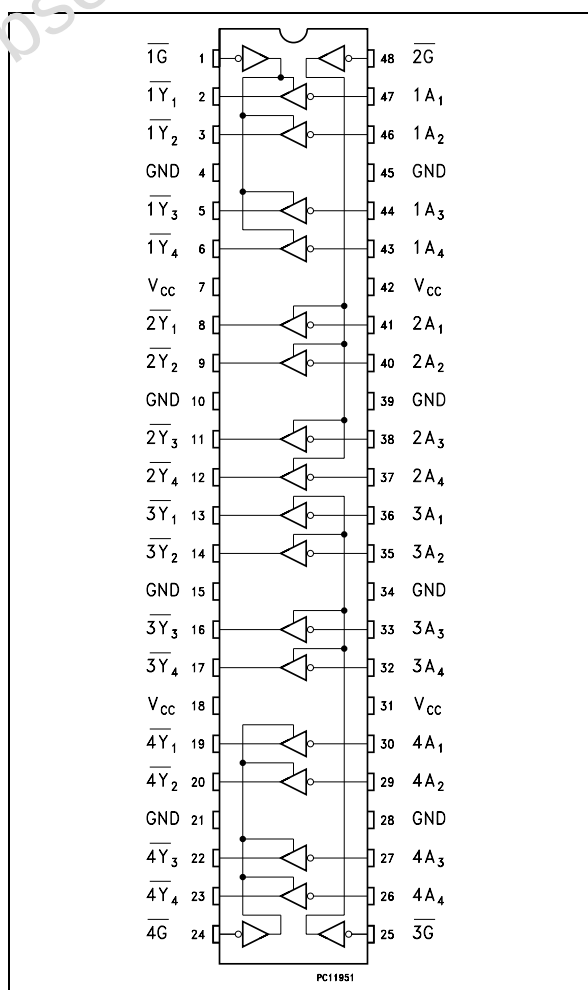
- HIGH SPEED: $t_{PD} = 5.3 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A = 25^\circ C$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPR)} = 2V$ to $5.5V$
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP} = 0.9V$ (MAX.)



ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74VHC16240TTR

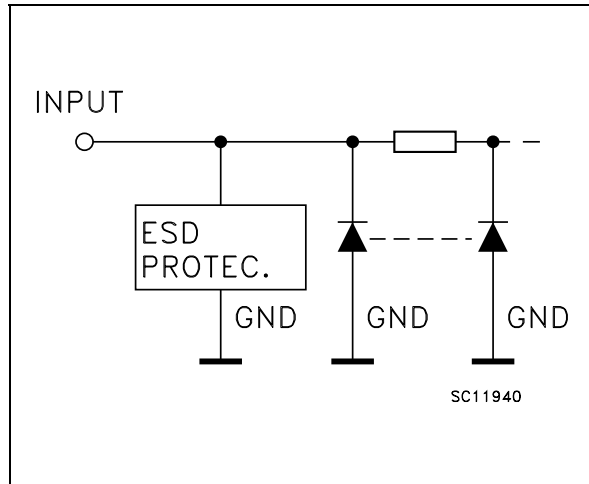
PIN CONNECTION



DESCRIPTION

The 74VHC16240 is an advanced high-speed CMOS 16-BIT BUS BUFFER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. Any $\overline{nG}$ output control governs four BUS BUFFERS. Output Enable inputs ($\overline{nG}$) tied together give full 16 bit operation. When $\overline{nG}$ is LOW, the outputs are on. When $\overline{nG}$ is HIGH, the output are in high impedance state. This device is designed to be used with 3 state memory address drivers, etc. Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

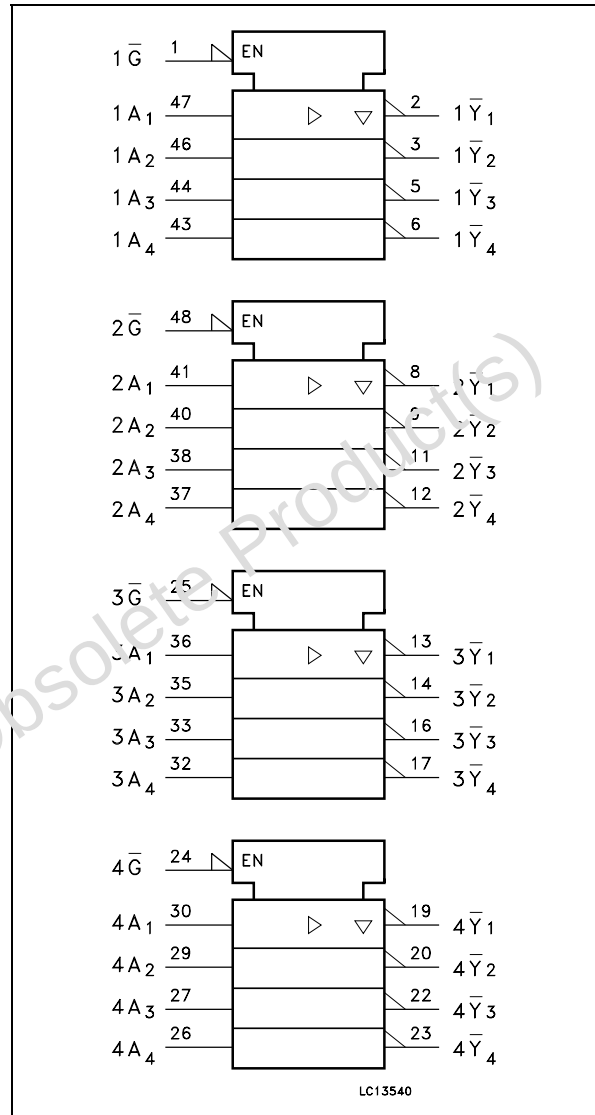
PIN No	SYMBOL	NAME AND FUNCTION
1	1G	Output Enable Input
2, 3, 5, 6	1Y ₁ to 1Y ₄	Data Outputs
8, 9, 11, 12	2Y ₁ to 2Y ₄	Data Outputs
13, 14, 16, 17	3Y ₁ to 3Y ₄	Data Outputs
19, 20, 22, 23	4Y ₁ to 4Y ₄	Data Outputs
24	4G	Output Enable Input
25	3G	Output Enable Input
30, 29, 27, 26	4A ₁ to 4A ₄	Data Input
36, 35, 33, 32	3A ₁ to 3A ₄	Data Input
41, 40, 38, 37	2A ₁ to 2A ₄	Data Input
47, 46, 44, 43	1A ₁ to 1A ₄	Data Input
48	2G	Output Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS		OUTPUT
$\overline{G}$	A _n	$\overline{Y_n}$
L	L	H
L	H	L
H	X	Z

X : Don't Care
Z : High Impedance

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 75	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 1) ($V_{CC} = 3.3 \pm 0.5V$) ($V_{CC} = 5.0 \pm 0.5V$)	0 to 100 0 to 20	ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		3.0 to 5.5		0.7V _{CC}			0.7V _{CC}		0.7V _{CC}			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		3.0 to 5.5				0.3V _{CC}		0.3V _{CC}		0.3V _{CC}		
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		1.9		V	
		3.0	I _O =-50 μA	2.9	3.0		2.9		2.9			
		4.5	I _O =-50 μA	4.4	4.5		4.4		4.4			
		3.0	I _O =-4 mA	2.58			2.48		2.4			
		4.5	I _O =-8 mA	3.94			3.8		3.7			
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1		0.1	V	
		3.0	I _O =50 μA		0.0	0.1		0.1		0.1		
		4.5	I _O =50 μA		0.0	0.1		0.1		0.1		
		3.0	I _O =4 mA			0.36		0.44		0.55		
		4.5	I _O =8 mA			0.36		0.44		0.55		
I _{OZ}	High Impedance Output Leakage Current	5.5	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.25		± 2.5		± 2.5	μA	
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			± 0.1		± 1		± 1	μA	
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40		40	μA	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

Symbol	Parameter	Test Condition			Value						Unit	
		V _{CC} (V)	C _L (pF)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time	3.3 ^(*)	15			5.3	8.4	1.0	10.0	1.0	10.0	ns
		3.3 ^(*)	50			7.8	11.9	1.0	13.5	1.0	13.5	
		5.0 ^(**)	15			3.6	6.0	1.0	6.5	1.0	7.0	
		5.0 ^(**)	50			5.1	8.0	1.0	8.5	1.0	9.0	
t _{PZL} t _{PZH}	Output Enable Time	3.3 ^(*)	15	R _L = 1KΩ		6.6	10.6	1.0	12.5	1.0	12.5	ns
		3.3 ^(*)	50	R _L = 1KΩ		9.1	14.1	1.0	16.0	1.0	16.0	
		5.0 ^(**)	15	R _L = 1KΩ		4.7	7.3	1.0	8.5	1.0	8.5	
		5.0 ^(**)	50	R _L = 1KΩ		6.2	9.3	1.0	10.5	1.0	10.5	
t _{PLZ} t _{PHZ}	Output Disable Time	3.3 ^(*)	50	R _L = 1KΩ		10.3	14.0	1.0	16.0	1.0	16.0	ns
		5.0 ^(**)	50	R _L = 1KΩ		6.7	9.2	1.0	10.5	1.0	10.5	
t _{OSLH} t _{OSHL}	Output to Output Skew time (note 1)	3.3 ^(*)	50				1.5		1.5		1.5	ns
		5.0 ^(**)	50				1.0		1.0		1.0	

(*) Voltage range is $3.3\text{V} \pm 0.3\text{V}$ (**) Voltage range is $5.0\text{V} \pm 0.5\text{V}$ Note 1 : Parameter guaranteed by design. $t_{soLH} = |t_{pLHm} - t_{pLHn}|$, $t_{soHL} = |t_{pHLm} - t_{pHLn}|$ **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition	Value							Unit
			T _A = 25°C			-40 to 85°C		-55 to 125°C		
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
C _{IN}	Input Capacitance			6	10		10		10	pF
C _{OUT}	Output Capacitance			8						pF
C _{PD}	Power Dissipation Capacitance (note 1)			20						pF

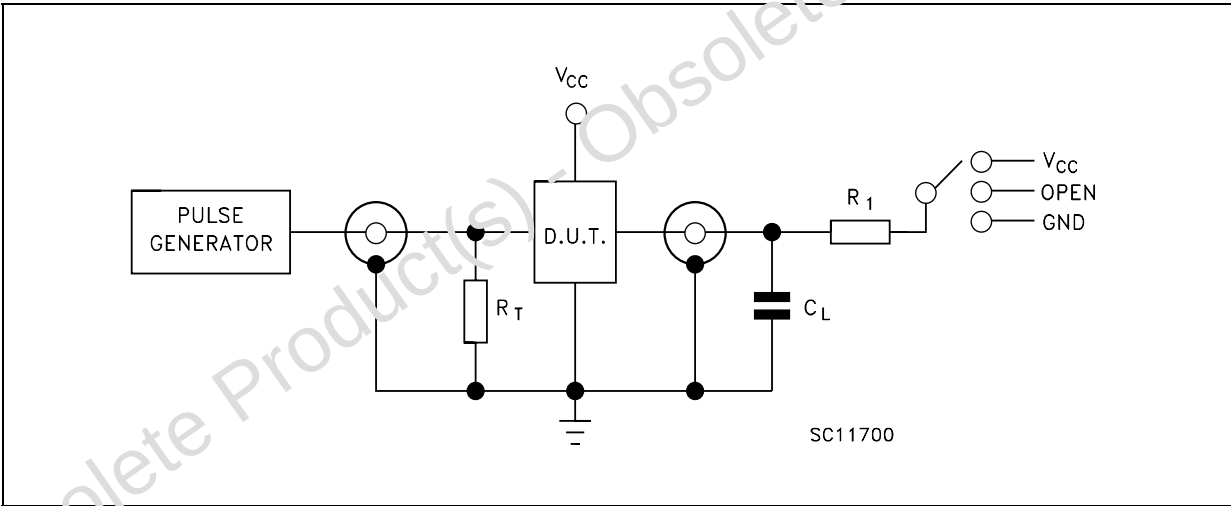
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per circuit)

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C _L = 50 pF		0.6	0.9					V
V _{OLV}				-0.9	-0.6						
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		3.5							V
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0					1.5				

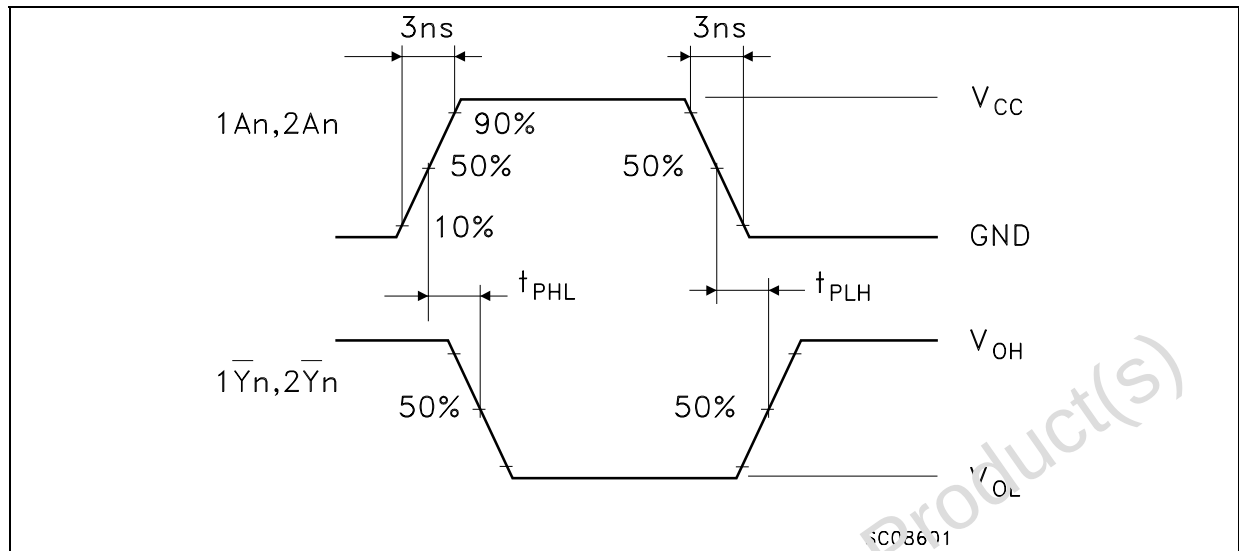
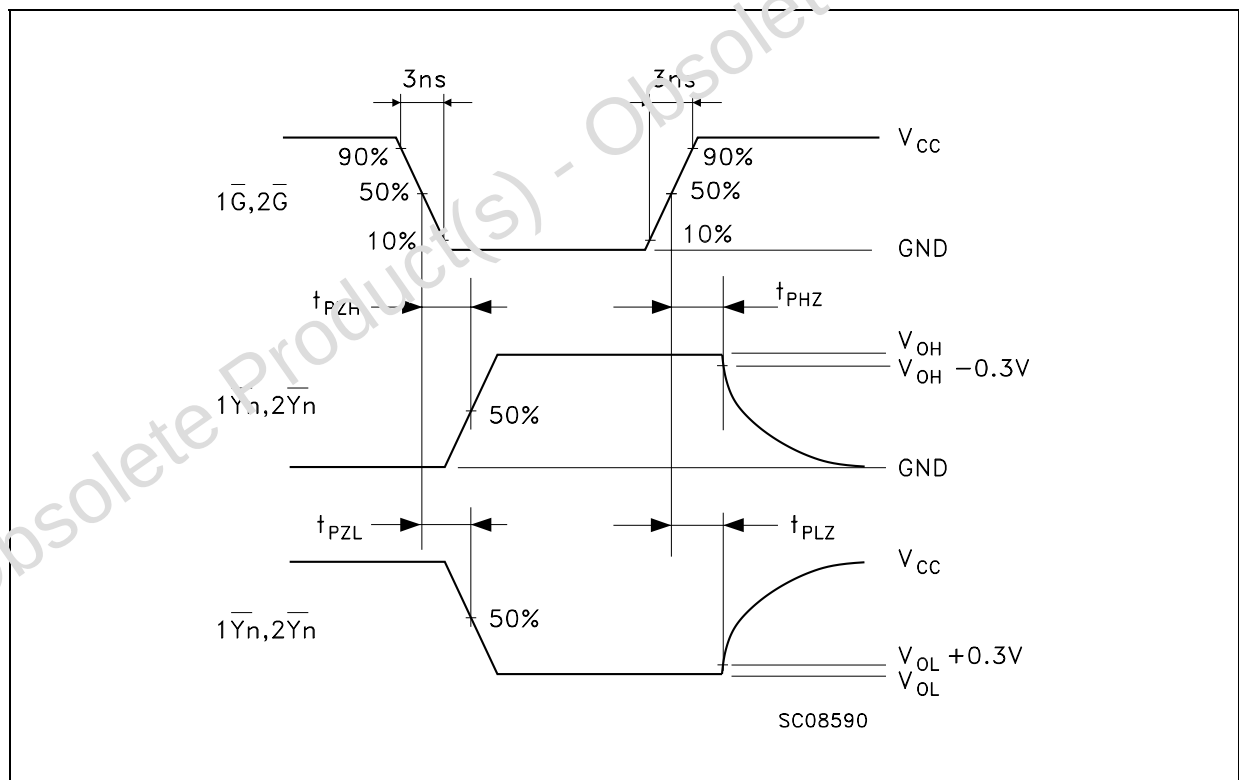
- 1) Worst case package.
2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.
3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

TEST CIRCUIT



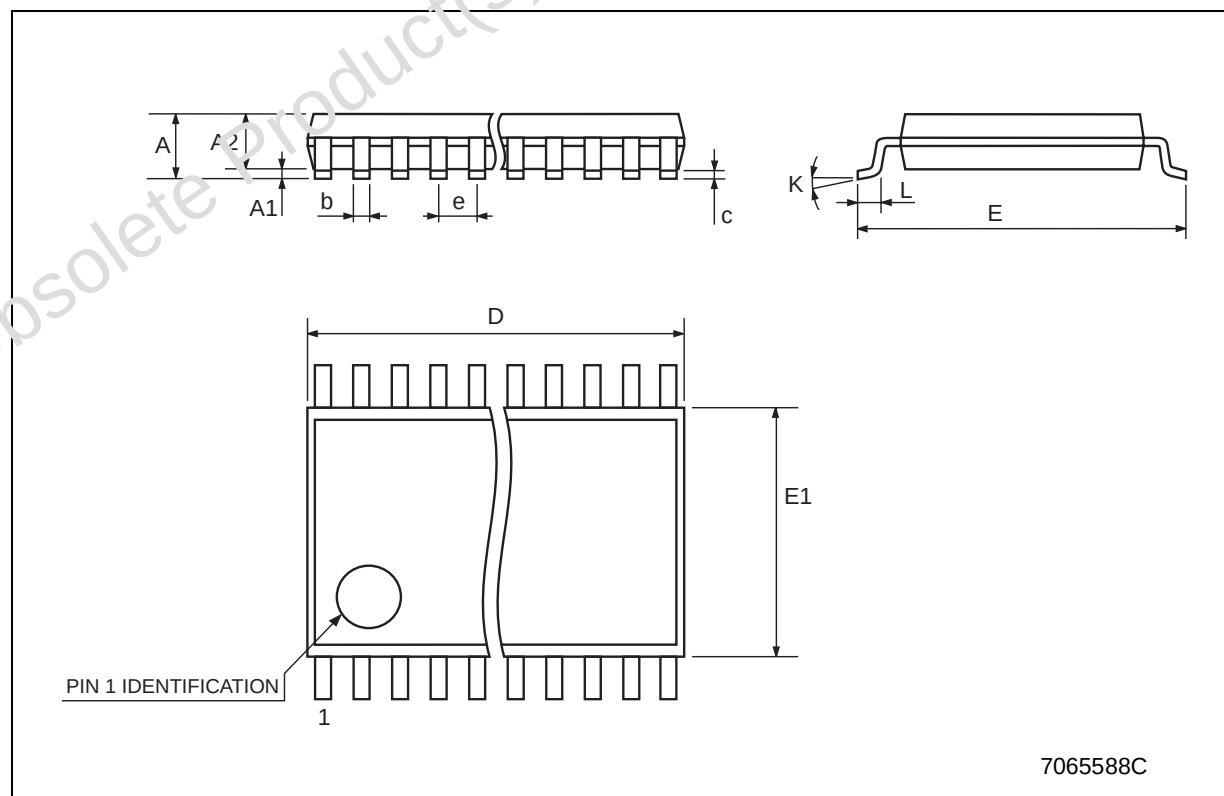
TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	V _{CC}
t _{PZH} , t _{PHZ}	GND

C_L = 15/ 50pF or equivalent (includes jig and probe capacitance)
R_L = R₁ = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1 : PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME** ($f=1\text{MHz}$; 50% duty cycle)

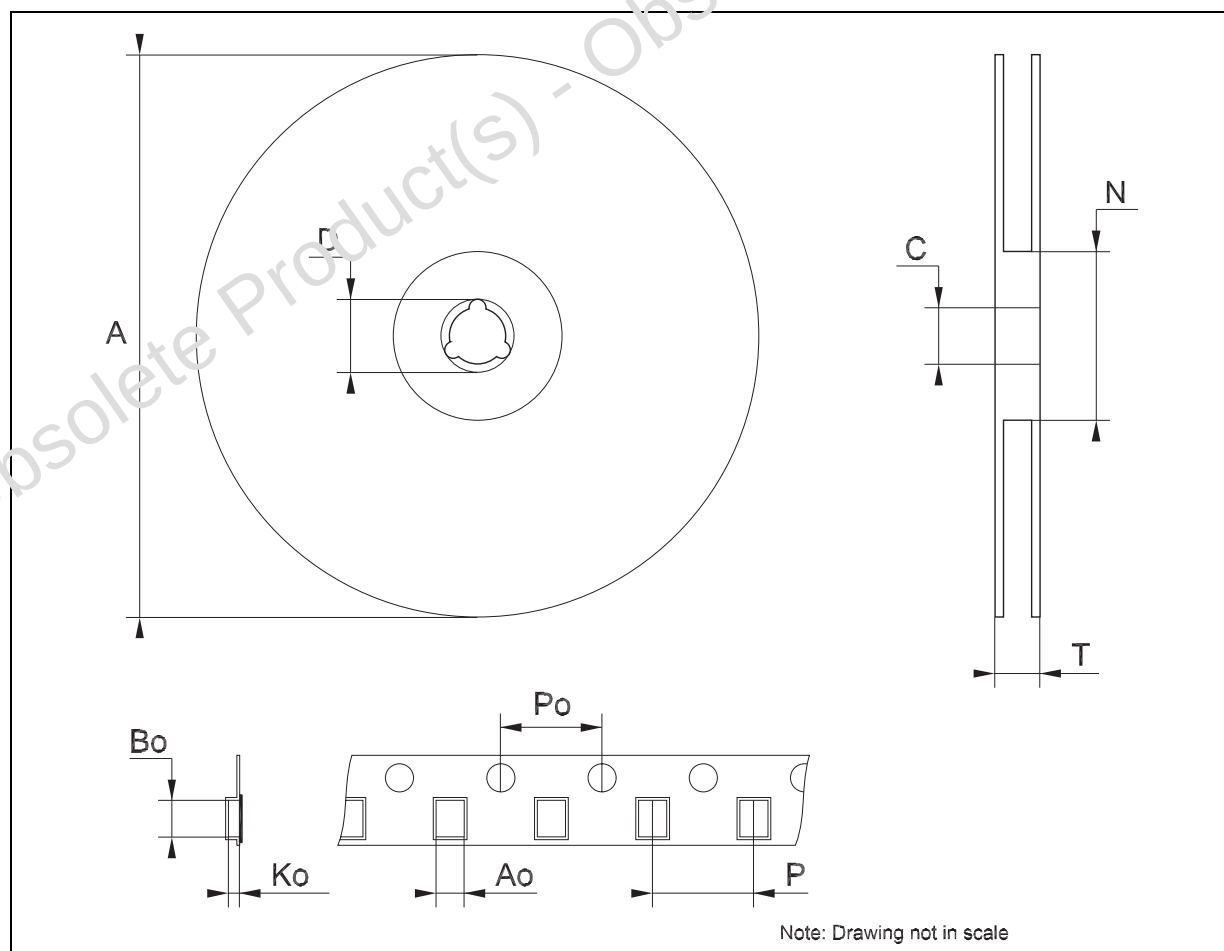
TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



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